form including all of the limitations of base claim 6. Accordingly, Claim 19 stands allowable.

Claim 36 stands rejected under 35 U.S.C. 102(b) as being anticipated by Nissen et al, US Patent No. 4,491,977. Applicants respectfully traverse this rejection.

Since Claim 36 has been rejected under 35 U.S.C. § 102(b), in order that the rejection of Claim 36 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court stated, "The identical invention must be shown in as complete detail as is contained in the ... claim". As set forth below, each and every element of Claim 36 is not set forth, either expressly or inherently described, in the Nissen reference.

Independent Claim 36, as amended, requires and positively recites, an apparatus, comprising: "a first processor comprising a core, a program memory and **a local memory**", "a second processor, **of a design other than said first processor**, comprising a core, a program memory and **a local memory**", "**a synchronizing circuit for coupling said first processor to said second processor**" and "one and only one common memory **coupling said first processor to said second processor**".

In contrast, Nissen clearly discloses that microprocessors 10a-10d do not include local memories 12a-12d (see Fig. 3 where local memory 10a is clearly outside the dashed line representing microprocessor 10a) – the memory is described as being "associated" with the microprocessor (col. 2, lines 44-45). Accordingly, Nissen's microprocessor does not comprise "**a local memory**", as required by Claim 36.

Next, since microprocessors 10a-10d are identical, Nissen fails to teach or suggest, "a second processor, **of a design other than said first processor**, comprising a core, a program memory and a **local memory**", as required by Claim 36.

Further, Nissen discloses that bus arbitration and control 28 in microprocessor 10a "in conjunction with all other identical central processor bus arbitration and control units, determines if this central processor unit is entitled to use the global bus" (col. 4, lines 25-29) – NOT to couple microprocessor 10a to another microprocessor (10b-10d). Accordingly, Nissen fails to teach or suggest, "a synchronizing circuit **for coupling said first processor to said second processor**", as required by Claim 36.

Further, being that only one bus arbitration and control 28 can use the global bus at any one time, Applicants respectfully submit that no two of microprocessors 10a-10d are ever coupled together. Moreover, even if it were possible to couple two of microprocessors 10a-10d together, arguendo, it would require TWO bus arbitration and controls 28 – NOT just one, as is required in Claim 36.

Lastly, while Nissen discloses that common memory 14 is coupled to microprocessors 10a-10d, it does NOT COUPLE two microprocessors 10 together – they are coupled together regardless of common memory 14. Accordingly, Nissen fails to teach "one and only one common memory **coupling said first processor to said second processor**", as required by Claim 36. As a result, the 35 U.S.C. 102(b) rejection of Claim 36 is overcome.

Claims 36-39 stand rejected under 35 U.S.C. 102(b) as being anticipated by Finch et al., US Patent No. 4,783,778. Applicants respectfully traverse this rejection.

Since Claims 36-39 has been rejected under 35 U.S.C. § 102(b), in order that the rejection of Claims 36-39 be sustainable, it is fundamental that "each and every element as set forth in the claims be found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir.

1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court stated, "The identical invention must be shown in as complete detail as is contained in the ... claim". As set forth below, each and every element of Claims 36-39 are not set forth, either expressly or inherently described, in the Finch reference.

Independent Claim 36, as amended, requires and positively recites, an apparatus, comprising: "a first processor comprising a core, a program memory and a local memory", "a second processor, **of a design other than said first processor**, comprising a core, a program memory and a local memory", "**a synchronizing circuit for coupling said first processor to said second processor**" and "one and only one common memory coupling said first processor to said second processor".

Independent Claim 37 requires and positively recites, an apparatus, comprising: "a main processor comprising a core, a program memory and a local memory", "a protocol processor, **of a design other than said main processor**, comprising a core, a program memory and a local memory", "**a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor**" and "one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 38 requires and positively recites, an apparatus, comprising: "a main processor comprising a core, a program memory and a local memory", "a protocol processor, comprising a core, a program memory and a local memory, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, an apparatus, comprising: "a main processor comprising a core, a program memory and a local memory", "a protocol

processor comprising a core, a program memory and a local memory, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited"**, "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor".

In contrast, Finch discloses that both processor A and processor B are "2MHz 65SC102 microprocessors which are responsible for transferring data between the microprocessors memory and I/O devices" (col. 6, lines 34-37). Accordingly, Finch fails to teach or suggest, "a second processor, **of a design other than said first processor**, comprising a core, a program memory and a local memory", as required by Claim 36, or "a protocol processor, **of a design other than said main processor**, comprising a core, a program memory and a local memory", as required by Claim 37, "a protocol processor, comprising a core, a program memory and a local memory, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited"**, as required by Claim 38, or "a protocol processor comprising a core, a program memory and a local memory, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited"**, as required by Claim 39.

The fact that Finch chose to have his identical processors A and B perform somewhat different tasks, does not change the reality that processors A and B are of the SAME DESIGN – accordingly, both processors A and B are "suited" to perform the same tasks. As a result, the 35 U.S.C. 102(b) rejection of Claims 36-39 is overcome.

Claims 6-7, 9-15, 17 and 36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al. (4,964,035) in view of Asano et al., (5,237,686). Applicants respectfully traverse this rejection.

Independent Claim 6 requires and positively recites, "a first processor for performing scalar processing, said first processor comprising a core, **a program memory and a local memory**", "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "a memory circuit **for coupling said local memory of said first processor to said local memory of said second processor**".

Independent Claim 36 requires and positive recites, "a first processor comprising a core, **a program memory and a local memory**", "a second processor, **of a design other than said first processor,** comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said first processor to said local memory of said second processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated May 15, 2001, page 5, lines 1-4). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated May 15, 2001, page 5, lines 4-7).

Applicants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin

processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. If the Examiner can identify such circuit, Applicants respectfully request him to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 36, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing. Accordingly, the 35 U.S.C. 103 rejection of Claims 6 and 36 over a combination of Aoyama and Asano is overcome.

Response to Examiner's rebuttal (12) (Office Action dated November 28, 2001, pages 14 –15). Applicants respectfully traverses the Examiner determination. More particularly, the Examiner never addresses the distinction between Aoyama (which discloses one vector processor and one protocol processor) and Asano, which discloses two vector processors. The Examiner argues that the teachings of one can be lumped into the teaching of the other.

Nowhere does the Examiner produce evidence from the prior art supporting his above determination.

Applicants further challenge the Examiner's determination that "it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama **because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor**". Applicants respectfully request the Examiner to cite are for his above determination. Since, according to the Examiner, "the feature is very well known in any type of computer architecture field", it should be very easy for the Examiner to cite such evidence.

Response to Examiner's rebuttal (13) (Office Action dated November 28, 2001, page 15). Applicants respectfully point out that the Examiner did not respond to the points raised by Applicants in the second paragraph of page 9 of their last amendment (Office Action dated September 5, 2001). Applicants kindly request that the issue raised by Applicants be addressed.

Further, while Asano may well disclose a synchronizing circuit, it is for the processors to "access a common memory" (e.g., fig. 6, el. 71 controlling the plurality processors to access a common memory 62; and col. 12, lines 58-61) – NOT for coupling the core of the first processor to the core of the second processor.

Response to Examiner's rebuttal (14) (Office Action dated November 28, 2001, page 15). Applicants respectfully traverse the Examiner's determination that "Asano clearly discloses one and only one common memory coupling the local memory of the first processor to the local memory of the second processor". In reality, while Asano discloses in Fig. 6 a common memory 62 peripherally connected to DSPs 63a, 63b ... 63n. Applicants fail to see

where common memory 62 "couples" the local memory of any one of DSPs 63a, 63b ... 63n to another one of the DSPs – the DSPs are already coupled to each other. The Examiner's determination is supposition not supported by fact.

Claims 7, 9, 10-15 and 17 stand allowable as depending from allowable claims and include further limitation not taught or suggested by the references of record.

Claim 7 further defines the apparatus of Claim 6, wherein said second processor is the main processor of said apparatus. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. Moreover, since Asano fails to teach or suggest the use of a "main" processor with processors DMM1-DMMk, it fails to overcome the previously identified deficiency of the Aoyama reference.

Response to Examiner's rebuttal (15) (Office Action dated November 28, 2001, page 16). Applicants respectfully traverse the Examiner's determination that "Aoyama teaches or suggests wherein the second processor is the main processor of the apparatus". The Examiner cites col. 4, line 63, of Aoyama for support. In reality, col. 4, line 63 discloses a "vector processing system". In contrast to the Examiner assertion, Aoyama does not disclose the "vector processing system" is a "main processor".

Claim 9 further defines the apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP". The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 7.

Response to Examiner's rebuttal (16) (Office Action dated November 28, 2001, page 16). Applicants reaffirm the above argument.

Claim 10 further defines the apparatus of Claim 6, wherein said program memory of said first processor is ROM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 11 further defines the apparatus of Claim 6, wherein said local memory of said first processor is RAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 12 further defines the apparatus of Claim 6, wherein said program memory of said second processor is ROM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 13 further defines the apparatus of Claim 6, wherein said local memory of said second processor is RAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Response to Examiner's rebuttal (17) (Office Action dated November 28, 2001, pages 16-17). Applicants reaffirm above arguments in support of Claims 10-13.

Claim 14 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Response to Examiner's rebuttal (18) (Office Action dated November 28, 2001, pages 17-18). Applicants reaffirm above the argument in support of claim 14.

Claim 15 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Response to Examiner's rebuttal (19) (Office Action dated November 28, 2001, page 18). Applicants reaffirm the above argument in support of Claim 15. Additionally, Aoyama (col. 10, line 13-16 and Fig. 5) specifically describes "multiple" common memories 108(1), 108(2), 108(3) – NOT "a" common memory as required by the present invention.

Claim 17 further defines the apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. The Aoyama and Asano references fail to teach or suggest this further limitation in combination with the requirements of Claim 6.

Response to Examiner's rebuttal (20) (Office Action dated November 28, 2001, page 19). Applicants reaffirm the above argument in support of Claim 17. Moreover, while the present invention discloses "a synchronizing circuit". Further, Applicants have reviewed the support cited by the Examiner in Aoyama (e.g., col. 5, line 63 and et seq.), and cannot find any support for the Examiner's determination.

Claims 8 and 35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et. al., in view of Asano et al., further in view of Mano. Applicants respectfully traverse this rejection.

Claim 8 further defines the apparatus of Claim 7, wherein said first processor is a microprocessor. Claim 35 further defines the apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and a matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type.

The Examiner admits that Aoyama does not show the scalar processor as a microprocessor (Office Action dated May 15, 2001, page 7, line 18). Asano fails to teach or suggest a "scalar processor" or "a scalar processor that is a microprocessor". While Applicants agree with the Examiner that Mano discusses providing a processor into a microprocessor, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references as applied to Claims 6 and 7. Accordingly, the 35 U.S.C. 103 rejection is overcome.

Claims 34-35 and 37-39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et. al., in view of Asano et al., further in view of Applicants' admitted prior art. Applicants respectfully traverse this rejection.

Claim 34 further defines the apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried out by a DSP and the use of array processor type". Moreover Applicants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano. Accordingly, the 35 U.S.C. 103 rejection of Claim 34 is overcome.

Claim 35 further defines the apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and a matrix computation

which requires a more powerful structure than that of the DSP and which is generally of the array processor type. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of a n application or the management or functioning and tasks generally carried out by a DSP and the use of array processor type". Moreover Applicants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano. Accordingly, the 35 U.S.C. 103 rejection of Claim 35 is overcome.

Independent Claim 37 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor, **of a design other than said main processor**, comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

Independent Claim 38 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a protocol processor comprising a core, a program memory and a local memory, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, "a main processor comprising a core, a program memory and a local memory", "a protocol processor comprising a core, **a program memory and a local memory**, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated May 15, 2001, page 5, lines 1-4 & page 11, lines 14-17). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated May 15, 2001, page 5, lines 4-7 & page 11, lines 17-12).

Applicants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. Line 21). Accordingly, since each unit processor DMM1-DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. If the Examiner can identify such circuit, Applicants respectfully request him to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Applicants further point out that the Examiner admits that Aoyama and Asano "do not show the use of the first processor being a protocol processor", (Office Action dated May 15, 2001, page 12, lines 7-8). The Examiner relies upon Applicants' specification page 1, line 6 - page 2, line 11 for teaching that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art.

Applicants respectfully disagree with the Examiner interpretation of page 1, line 6 - page 2, line 11 of the instant specification. While "protocol processing" may itself be known in the art, there is no teaching or suggestion in Applicants' prior art that it could be combined with the teaching of Aoyama and Asano to obviate the present invention. Applicants further submit that the teaching of page 1, line 6 - page 2, line 11 of the instant specification does not overcome the previously identified deficiencies of the Aoyama and Asano references. Moreover Applicants admitted prior art does nothing to overcome the above-identified deficiencies of the Aoyama and Asano references, nor is there in teaching that suggests any combination of the admitted prior art with the teaching of Aoyama and Asano.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 37 & 39, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-

DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing, in combination with the teaching of page 1, line 6 - page 2, line 11 of the instant specification. Accordingly, the 35 U.S.C. 103 rejection of Claims 37-39 over a combination of Aoyama, Asano and Applicant's prior art is overcome.

Response to Examiner's rebuttal (21) (Office Action dated November 28, 2001, pages 20-21). While the Examiner has put forth his OWN theory that, "it would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation power and functionality", the Examiner has provided no evidence to support his determination.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest ALL the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on

applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner has not satisfied the above requirements.

Claims 34 and 37-39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et. al., in view of Asano et al., further in view of Finch. Applicants respectfully traverse this rejection.

Claim 34 further defines the apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. While Asano does disclose the use of DSPs to perform signal processing on video signals, it fails to teach or suggest the previously discussed deficiencies of the Aoyama and Asano references. It further fails to teach or suggest, "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried out by a DSP and the use of array processor type". Even if, arguendo, Finch discloses "a protocol processor performing protocol processing", Applicants' response is "so what"? Finch does not overcome the previously discussed deficiencies of Aoyama and Asano and there is no teaching or suggestion in Finch suggesting that it could be combined with the teachings of Aoyama and Asano in the manner suggested by the Examiner. Accordingly, the 35 U.S.C. 103 rejection of Claim 34 is overcome.

Independent Claim 37 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor, **of a design other than said main processor**, comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

Independent Claim 38 requires and positively recites, "a **main processor** comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core, a program memory and a local memory, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core, a **program memory and a local memory**, said protocol processor **being of a design which enables said protocol processor to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

The Examiner admits that Aoyama "does not show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor" (Office Action dated May 15, 2001, page 5, lines 1-4 & page 11, lines 14-17 & page 14, lines 13-16). The Examiner relies upon Asano as "teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory" (Office Action dated May 15, 2001, page 5, lines 4-7 & page 11, lines 17-12 & page 14, lines 16-20).

Applicants respectfully traverse the Examiner's interpretation of Asano and point out that Asano's processor DMM1-DMMk (11a-11k) are ALL digital signal processors (Figs. 1 & 2; Col. 9, lines 46-53) which are used exclusively for video signal processing (col. 5, lines 50-55; col. 6. lines 57- col. 8. Line 21). Accordingly, since each unit processor DMM1-

DMMk is in charge of processing image signals for a plurality of sectional frames which are not contiguous but separated from each other, and all the unit processor simultaneously begin processing in synchronism with the state of a new picture frame, each of processors DMM1-DMMk appear to perform "vector" processing, and not "scalar" processing. Accordingly, it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Asano similarly fails to teach or suggest a "synchronizing circuit for coupling said core of said first processor to said core of said second processor", as required by Claims 6 and 36. If the Examiner can identify such circuit, Applicants respectfully request him to do so. This is yet another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing.

Applicants further point out that the Examiner admits that Aoyama and Asano "do not show the use of the first processor being a protocol processor", (Office Action dated May 15, 2001, page 12, lines 7-8 & page 15, lines 6 & 7). The Examiner relies upon Finch (col. 8, line 42 and et seq.) for teaching that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art.

Applicants respectfully disagree with the Examiner interpretation of page 1, line 6 - page 2, line 11 of the instant specification. While "protocol processing" may itself be known in the art, there is no teaching or suggestion in Applicants' prior art that it could be combined with the teaching of Aoyama and Asano to obviate the present invention. Applicants fail to understand how adding the teaching of page 1, line 6 - page 2, line 11 of the instant specification overcomes the previously identified deficiencies of the Aoyama and Asano references.

Asano further fails to teach or suggest, "one and only one common memory coupling the local memory of the first processor to the local memory of the second processor", as required by Claim 37 & 39, since Asano clearly discloses "multiple" common memories 10a-10n coupling processors DMM1-DMMk (Figs. 1 & 2). This is yet still another reason why it would not have been obvious to one having ordinary skill in the art at the time of the invention to have combined the teaching of Asano (which discloses processors DMM1-DMMk for "vector" processing) into Aoyama which discloses one processor for "scalar" processing and one for "vector" processing, in combination with the teaching of page 1, line 6 - page 2, line 11 of the instant specification. Accordingly, the 35 U.S.C. 103 rejection of Claims 37-39 over a combination of Aoyama, Asano and Finch is overcome.

Objected to Claim 19 has been amended to be allowable. Claims 6-15, 17 and 34-39 stand allowable over the cited art and the application is in allowable form. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418